IN THE SPECIFICATION:

Following the Title of the application, please add the following section heading and paragraph:

--CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of application Serial No. 10/231,087 filed December 8, 2000, now United States Patent No. _____, which is incorporated herein in its entirety by reference thereto.--

Please replace the paragraph on page 4, lines 7 through 15 as follows:

FIG. 2 is a functional block diagram of a hardware block configuration, in accordance with an embodiment of the present invention. In FIG. 2, all critical memory structures 200 and 201on a processor are either protected by parity or ECC. On detecting an error, these structures will assert the error signals to the processor error processing logic 202. The processor error processing hardware will save the following information:

- The physical address (PA) of an offending operation (that is, the operation that caused the error) in an errant process physical address register 203
- The instruction pointer at the time the error is detected in an interruption instruction pointer (IIP) register 204.

Please replace the Abstract as follows:

The present invention relates to a method and system for efficiently identifying errant processes in a computer system using an operating system (OS) error recovery method that identifies if the error caused by the errant process can be recovered and, if so, can recover from the error. The method and system of the present invention operates after standard Error Correcting Code (ECC) and parity check bit methods and systems are unsuccessful in recovering from the error. In accordance with an embodiment of the present invention, the method and system includes detecting an error during instruction execution, storing a physical address of an

errant process that caused the error, and storing an execution instruction pointer (IP) in a processor including at least one critical memory structure to detect an error and a processor error processing logic hardware coupled to the at least one critical memory structure. The processor error processing logic hardware to store a physical address of an errant process that caused the error, store an execution instruction pointer (IP) in an interruption instruction pointer (IIP), determine a first virtual address from an operating system mapping table, determine a second virtual address from a translation look-aside buffer, and identify the errant process, if the physical address and the second virtual address match the physical address and the first virtual address.